Attorney's Docket No.:10559/364001/P8247X

Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1-33 (cancelled)

34. (previously presented): A data processing system, comprising:

a processor;

a main memory;

a multi-ported memory in communication with the processor and the main memory, the multi-ported memory having a storage capacity of about 4 kilobytes or greater; and

wherein the system is configured to receive a request to write information to a memory location, wherein the information has an information type equal to data or control information, and wherein the system is further configured to determine a memory destination between the main memory or the multi-ported memory based on the information type.

35. (previously presented): The system of claim 34, further comprising an operating system configured to determine the memory destination based on the information type.

Attorney's Docket No.:10559/364001/P8247X

3 1
36. (previously presented): The system of claim 34, wherein the system further includes:

D1

a peripheral device; and

a peripheral device controller, wherein the controller is configured to determine the memory destination based on the information type.

4 1
37. (previously presented): The system of claim 34, wherein the multi-ported memory is included in a memory controller.

5 1
38. (previously presented): The system of claim 34, wherein the multi-ported memory is dual-ported.

6 1
39. (previously presented): The system of claim 34, wherein the multi-ported memory and memory controller are integrated into a single chip.

7 1
40. (previously presented): The system of claim 34, wherein the multi-ported memory includes memory chosen from the group consisting of static random access memory and dynamic random access memory.

Attorney's Docket No.:10559/364001/P8247X

8

41. (previously presented): The system of claim 34, wherein the multi-ported memory stores reservation bits mapped to blocks of general-purpose memory in the multi-ported memory.

9

42. (previously presented): The system of claim 34, wherein virtual addresses within multi-ported memory are mapped to physical addresses with smart addressing.

10

43. (previously presented): The system of claim 34, further including:

a memory controller in communication with the main memory and the multi-ported memory; and

a peripheral device in communication with the memory controller via an input/output bus.

11

44. (previously presented): The system of claim 34, wherein for information with an information type equal to control information, the system is configured to determine the memory destination to be the multi-ported memory and not the main memory.

12

45. (previously presented): A method comprising:

receiving a request to write information to a memory location;

determining an information type equal to data or control information for the information; and

determining a memory destination between a main memory and a multi-ported memory based on the information type, the multi-ported memory having a storage capacity of about 4 kilobytes or greater.

13 12
~~46~~. (previously presented): The method of claim ~~45~~, further comprising:

writing the information to the memory destination based on the determining the memory destination.

14 12
~~47~~. (previously presented): The method of claim ~~45~~, wherein determining the memory destination between the main memory and the multi-ported memory based on the information type comprises determining the memory destination to be the multi-ported memory for the information type equal to control information.

15
~~48~~. (previously presented): An article comprising a computer-readable medium which stores computer-executable instructions, the instructions causing one or more machines to perform operations comprising:

receiving a request to write information to a memory location;

determining an information type equal to data or control information for the information; and

determining a memory destination between a main memory and a multi-ported memory based on the information type, the multi-ported memory having a storage capacity of about 4 kilobytes or greater.

16 15
~~49~~. (previously presented): The article of claim ~~48~~, further comprising:

writing the information to the memory destination based on the determining the memory destination.

17 15
~~50~~. (previously presented): The article of claim ~~48~~, wherein determining the memory destination between the main memory and the multi-ported memory based on the information type comprises determining the memory destination to be the multi-ported memory for the information type equal to control information.

Attorney's Docket No. 10559/364001/P8247-2

Sub A1 > ~~ACCESSING MULTI-PORTED MEMORY~~

This is a continuation in part of Ser. No. 09/572,047, which is abandoned on April 15, 2003. filed May 16, 2000. A

ck 2/21/05

BACKGROUND

This invention relates to accessing multi-ported memory.

In a conventional computing system the central processing unit (CPU), main memory and input/output (I/O) devices are connected by a bus. A "bus master" or "bus arbiter" controls and directs data traffic among the components of the computing system.

Main memory is used as the principal site for storing data. An "access" to main memory writes data to or reads data from main memory. Making an access (or "accessing") is typically preceded by a request for access from another component of the system, such as the CPU or an I/O device, followed by a grant of permission by the bus arbiter.

There are two principal types of accesses. The first type is a data access, in which large amounts of data are written to or read from main memory. A data access may be on the order of thousands of bytes. The second type is a control/status access, characterized by a small number of reads or writes to a defined data structure in order to report the status of an input/output device, process data, or

initiate some input/output activity. In contrast to data accesses, a control/status access is usually on the order of a few bits. Control accesses are generally initiated by the CPU, while status accesses are generally initiated by the I/O devices.

DESCRIPTION OF DRAWINGS

Figs. 1 and 2 are conceptual block diagrams depicting an embodiment of the invention.

Sub A2 7

Fig. 3 is a conceptual block diagram depicting a component shown in Fig. 2, illustrating an embodiment of the invention.

DETAILED DESCRIPTION

In Fig. 1, a computer architecture 10 includes a central processing unit (CPU) 12, main memory 22 and I/O devices 26. Main memory 22 is generally a form of random access memory (RAM), such as dynamic RAM (DRAM), Rambus™ DRAM (RDRAM), synchronous DRAM (SDRAM) or SyncLink DRAM (SLDRAM). Communications among these components are regulated by a memory controller 16. Memory controller 16 performs the functions of a bus arbiter by managing communications 14 with CPU 12, communications 20 with main memory 22, and communications 24 with I/O devices 26.